Implementation of Memory Centric Scheduling for COTS Multi-Core Real-Time Systems

Juan M. Rivas, Joël Goossens, **Xavier Poczekajlo**, Antonio Paolillo

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PARTS

Multi-core: a challenge?

[. . .] multi-core hardware raises substantial **challenges** *[. . .]* Maiza et al. 2018

This poses new **challenges** *for scheduling [. . .]*, Agrawal et al. 2017

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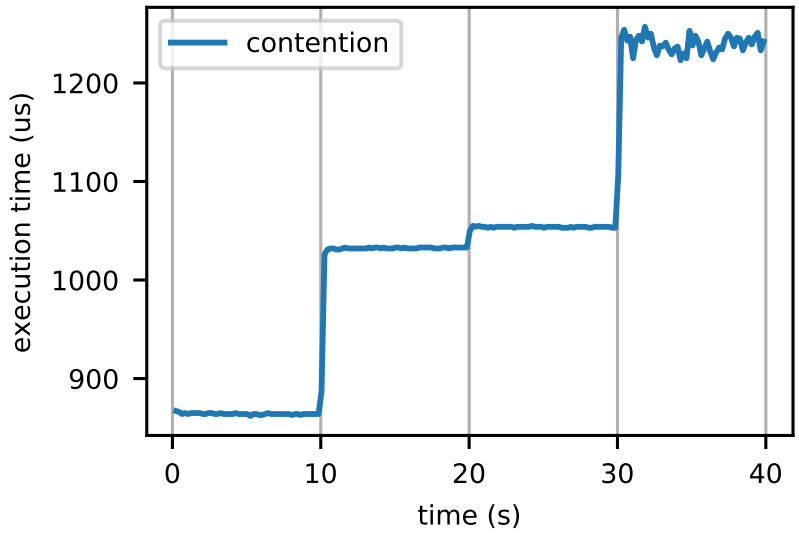

From 1 to 4 tasks

Existing approaches

- Time Division Multiple Access
- Memory Centric scheduling
- Bandwidth Regulator
- More advanced analysis
- ...

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- Time Division Multiple Access
- Memory Centric scheduling
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× Specialised hardware

× High analytical complexity

× Not implemented

Our work: Memory Centric

- ~~Specialised hardware~~ COTS

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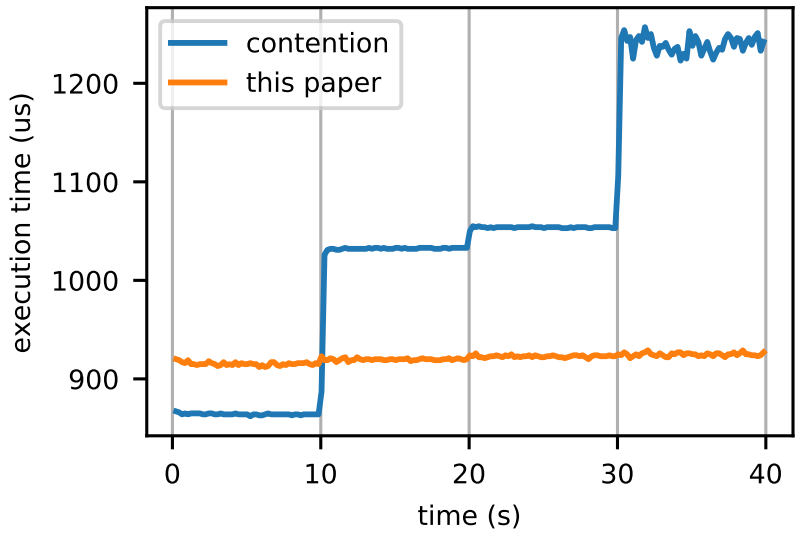

From 1 to 4 tasks

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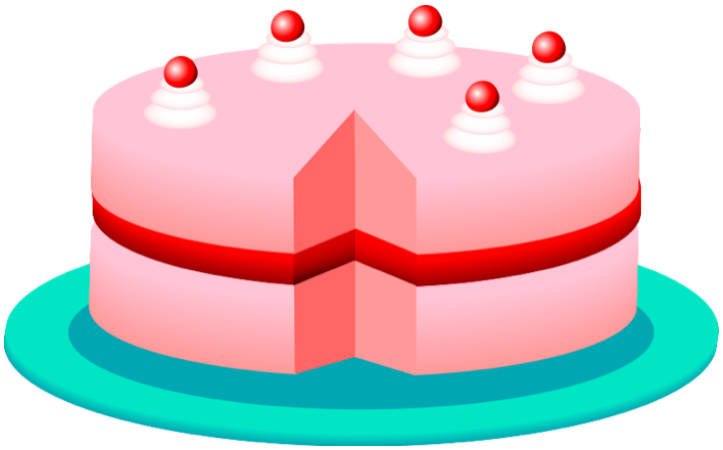
Memory Centric

Assumptions: data



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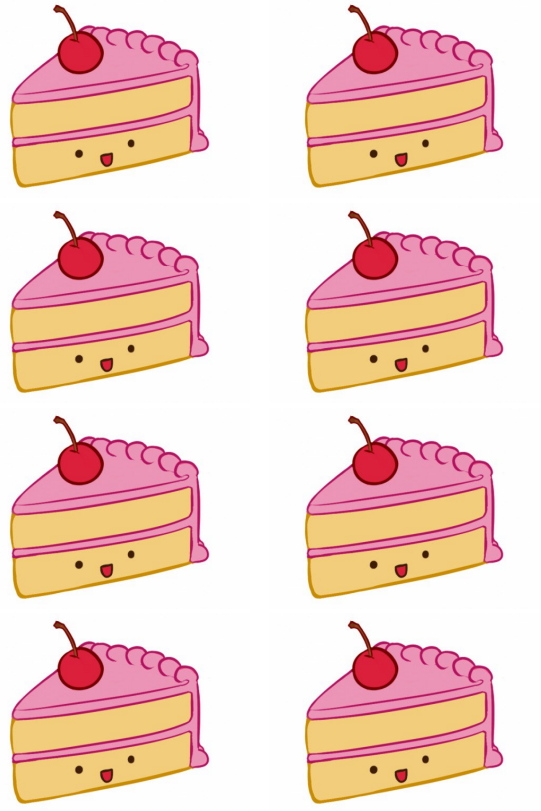
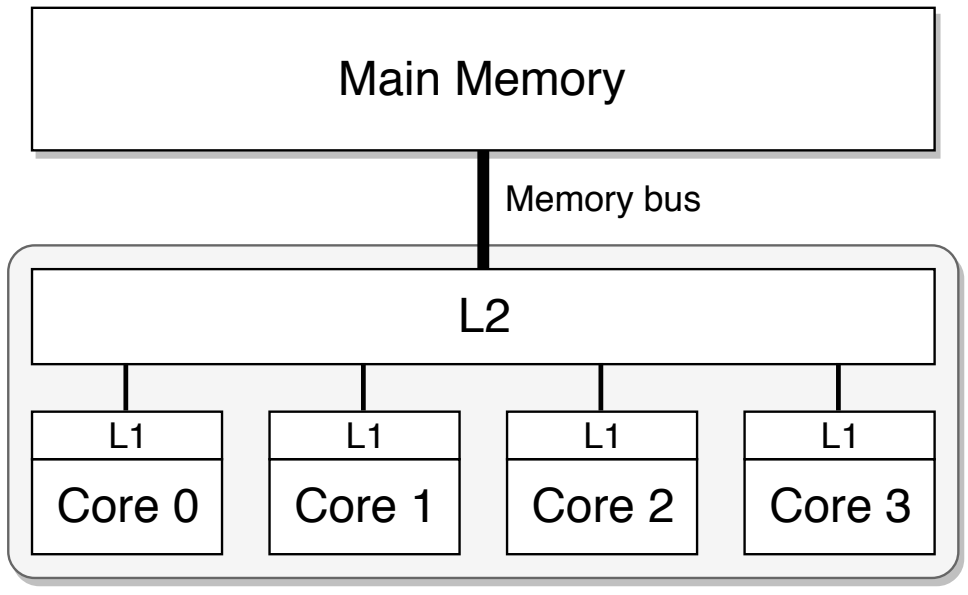
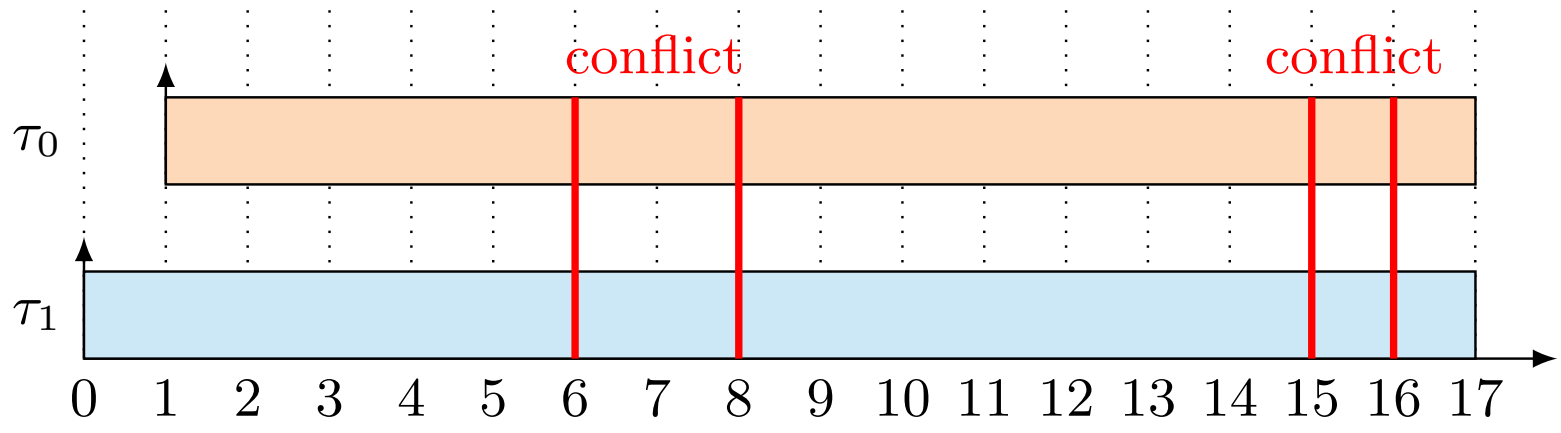


Assumptions: hardware

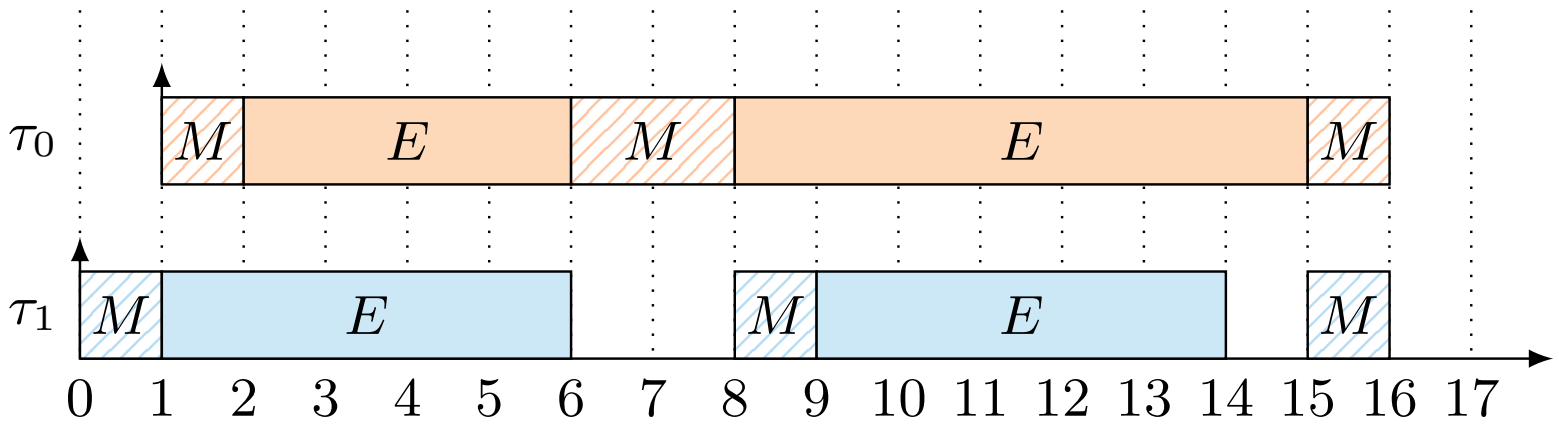


Contention vs Memory centric



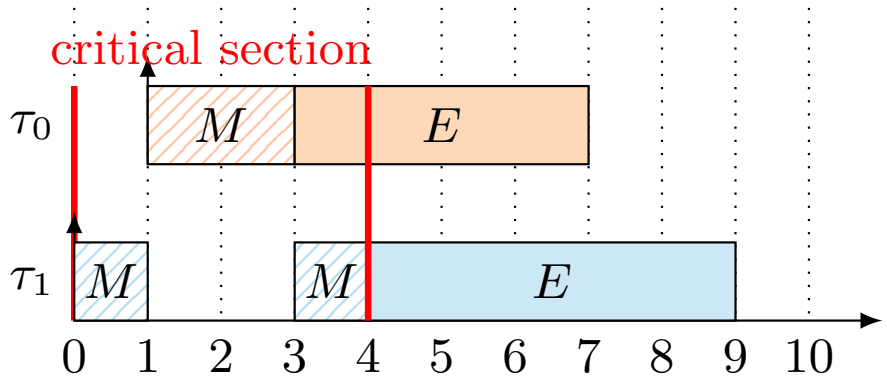
Contention approach

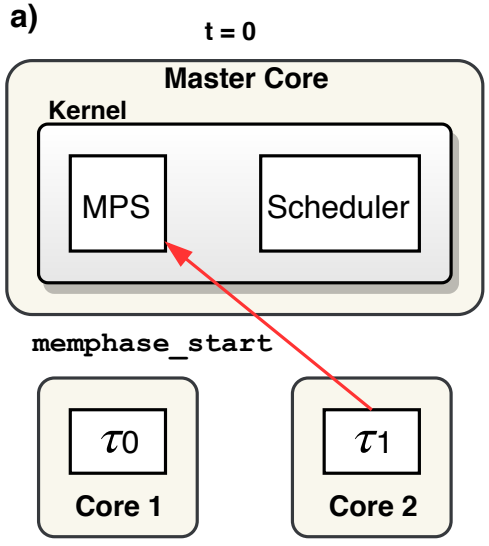
Contention vs Memory centric



Memory centric approach, $\tau_0 \succ \tau_1$

Critical section and preemptive mutex





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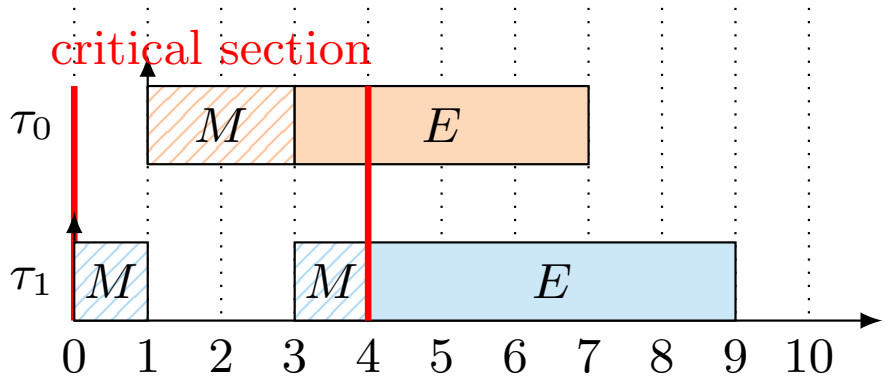

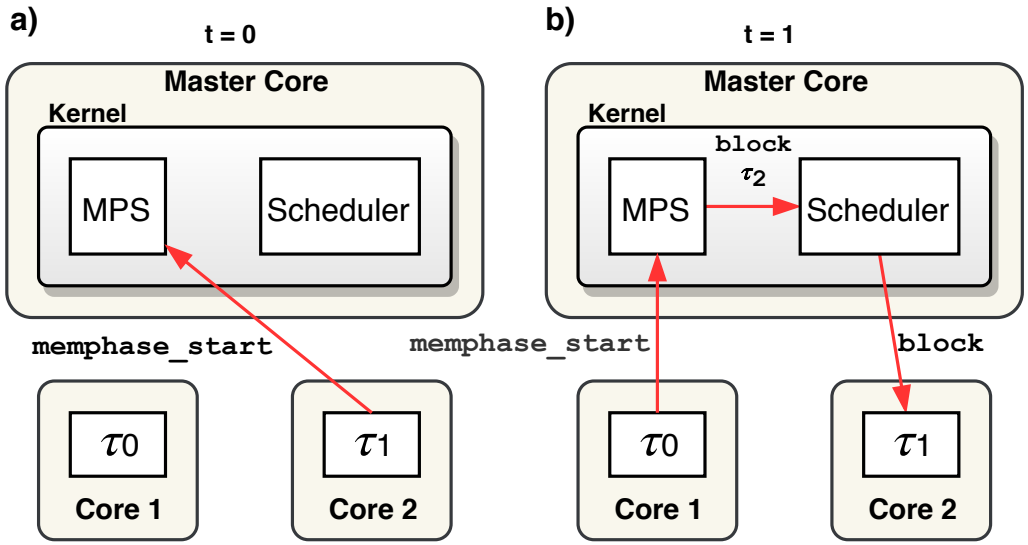

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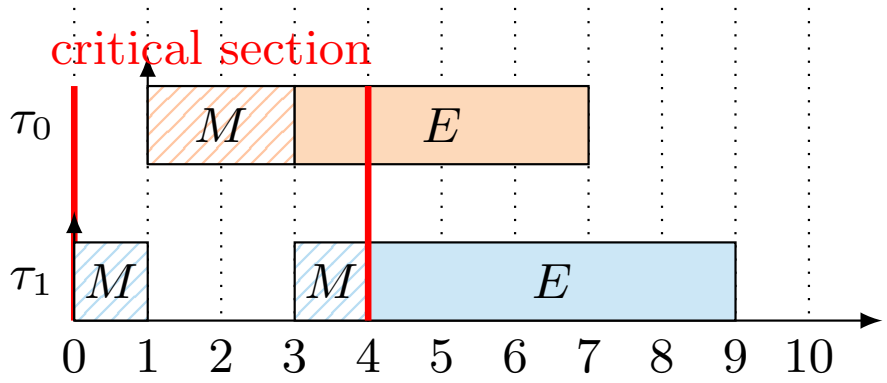
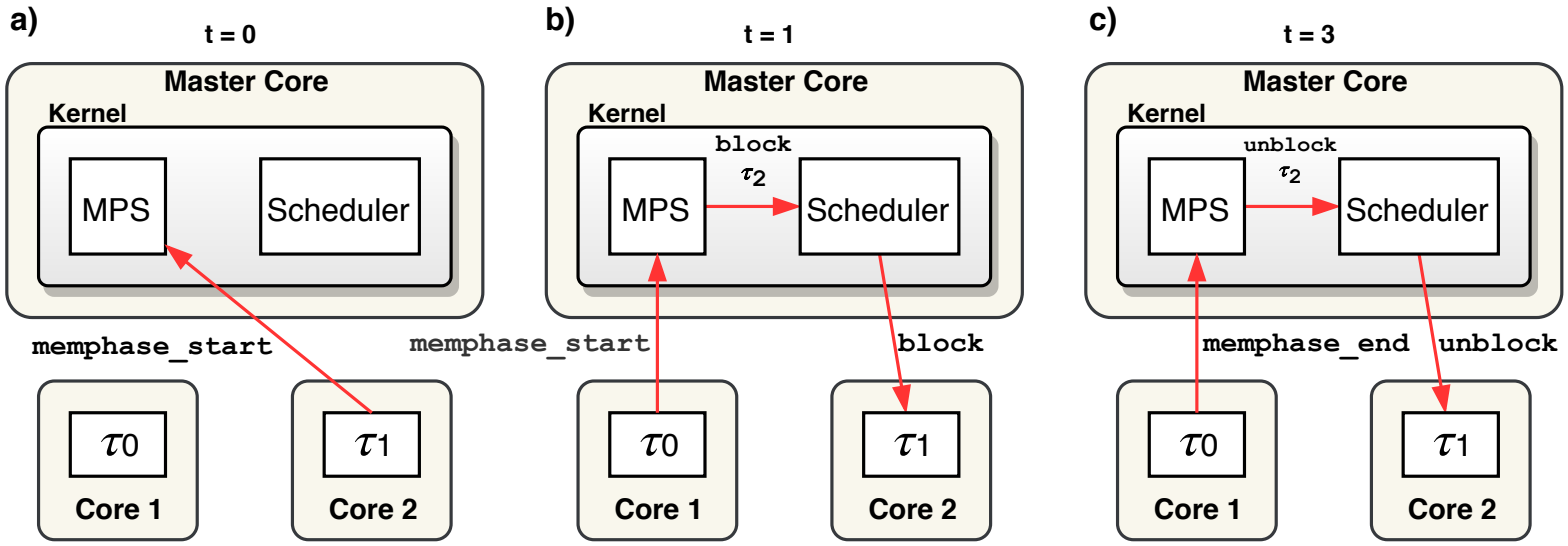
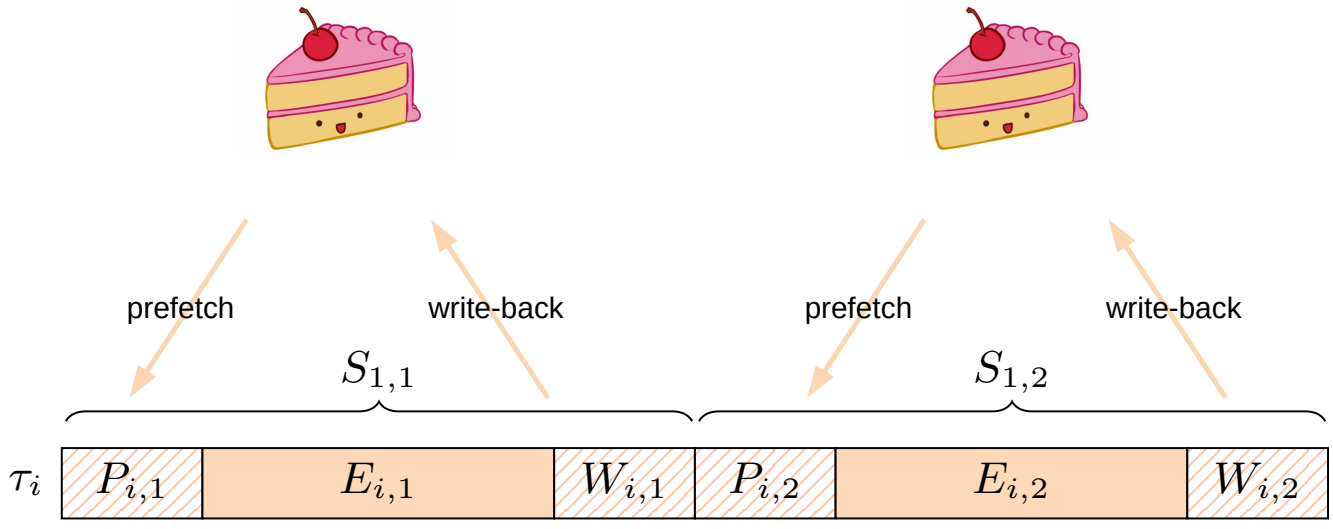
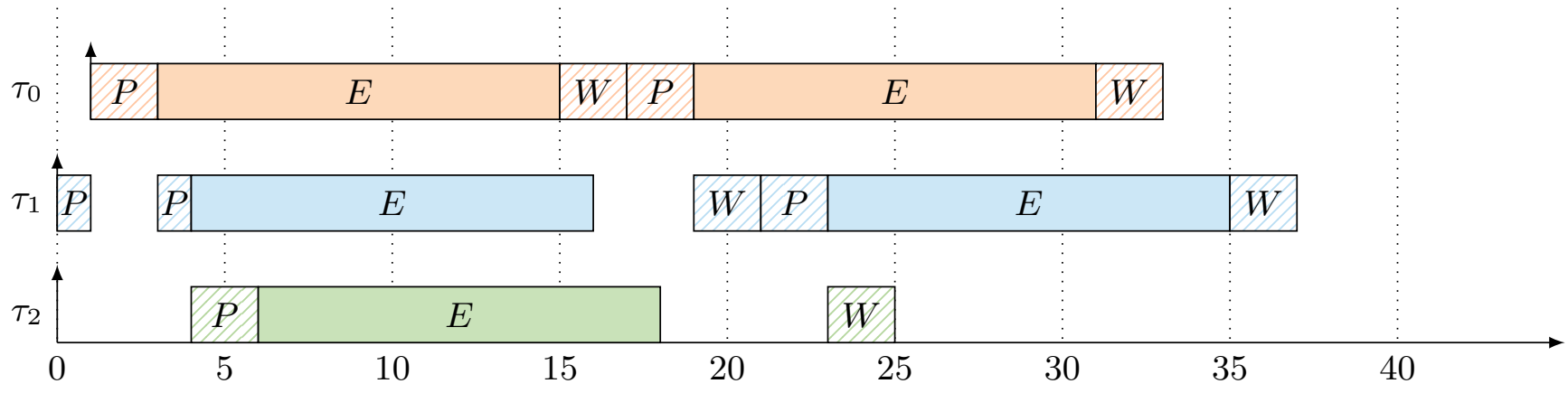




Adding semantics to memory phases

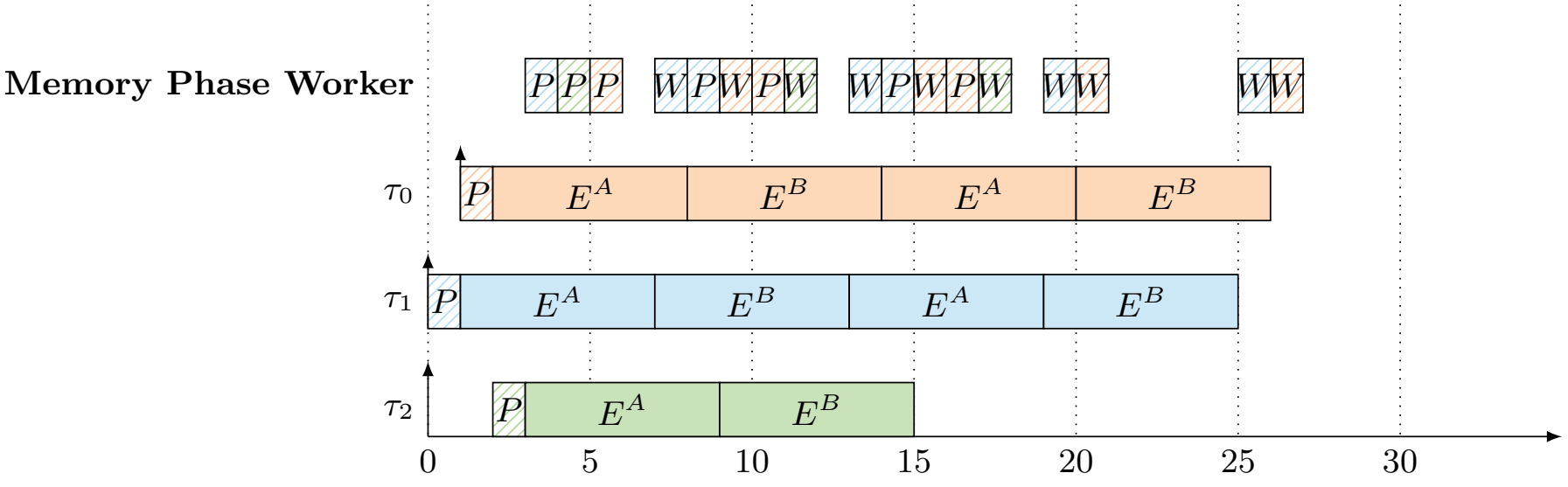


S-MP and A-MP approaches



Synchronous memory phases (S-MP), $\tau_0 \succ \tau_1 \succ \tau_2$

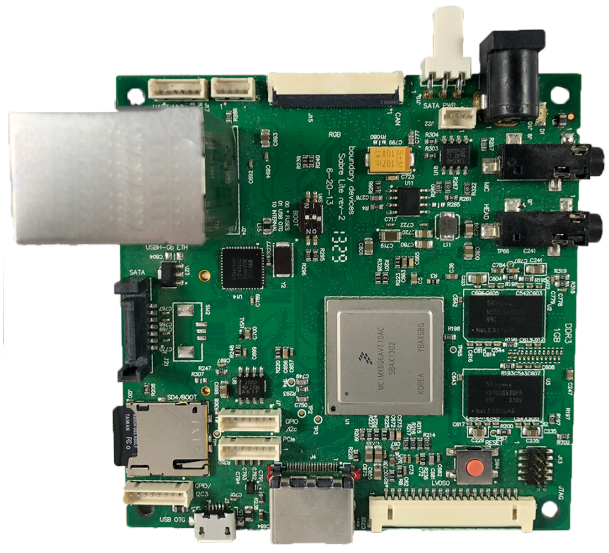
S-MP and A-MP approaches



Asynchronous memory phases (A-MP), $\tau_0 \succ \tau_1 \succ \tau_2$

Experimentation

Experimental setup



+

BD-SL-I.MX6
4 Cortex-A9 cores
1GB of DDR3 RAM

HIPPEROS

=

3 applications, 4 tasks, 430000 executions

Experimental setup

$= \quad 0.2\text{MB}$

$$\tau_0 \succ \tau_1 \succ \tau_2 \succ \tau_3$$

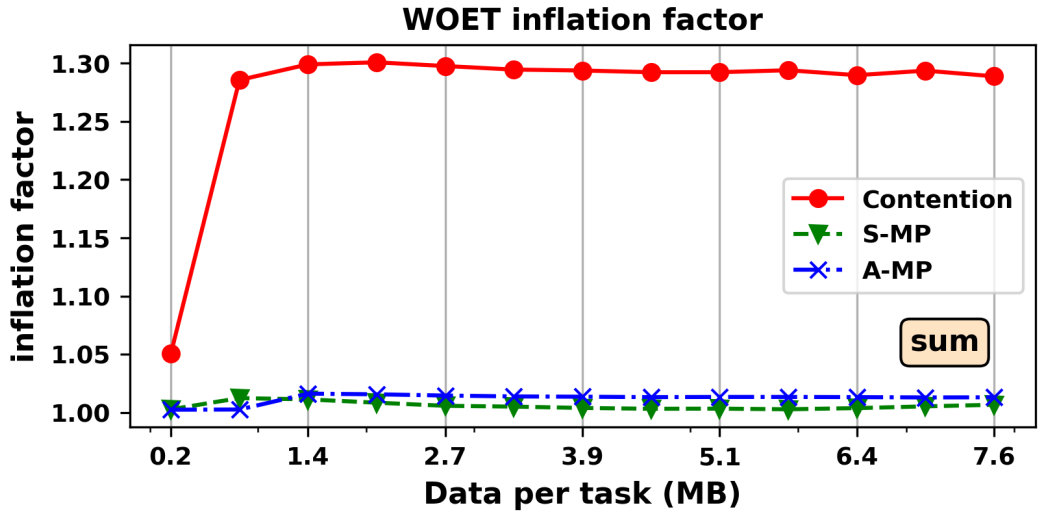
WOET Inflation factor τ_0

τ_0	$\emptyset$
$\emptyset$	$\emptyset$

WOET

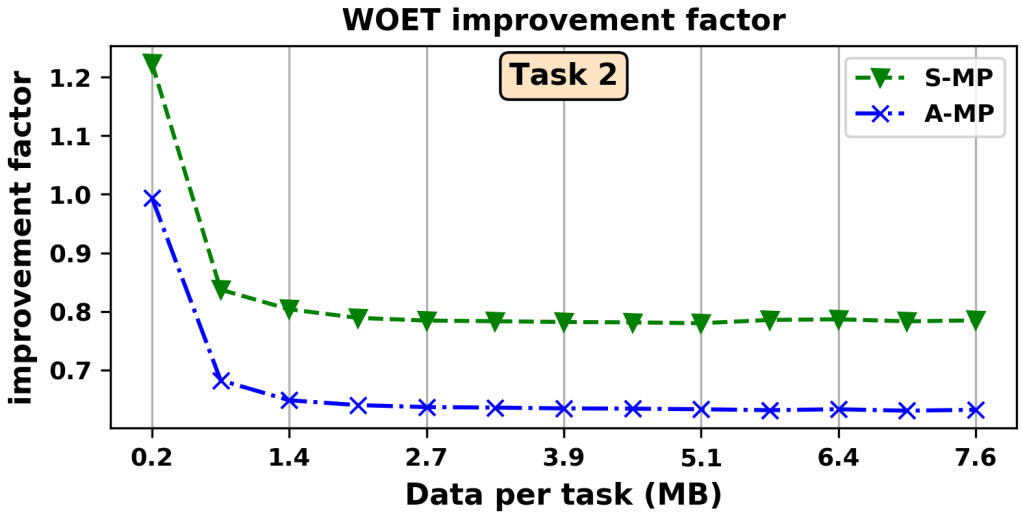
τ_0	τ_1
τ_2	τ_3

WOET



Improvement factor τ_2

$$\frac{\text{Mem. Centric WOET}}{\text{Contention WOET}}$$



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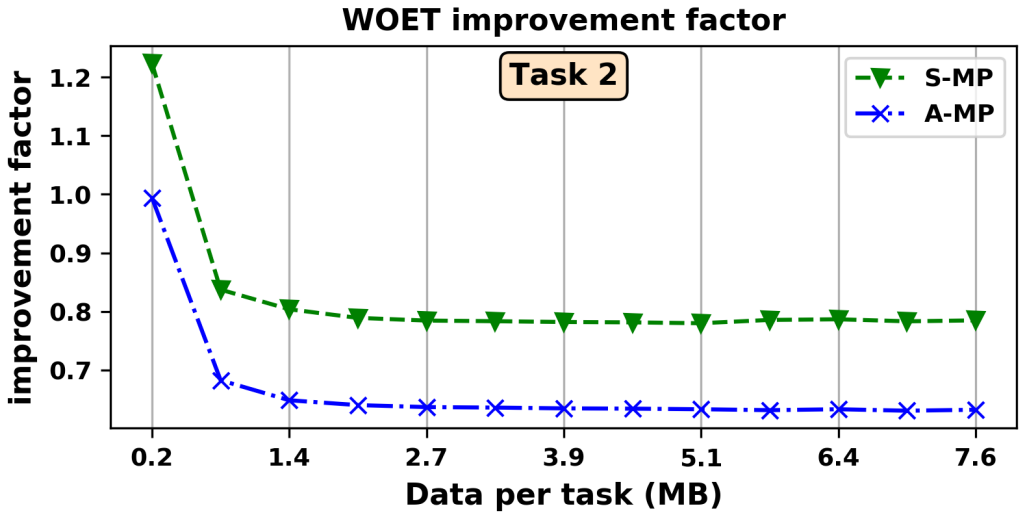
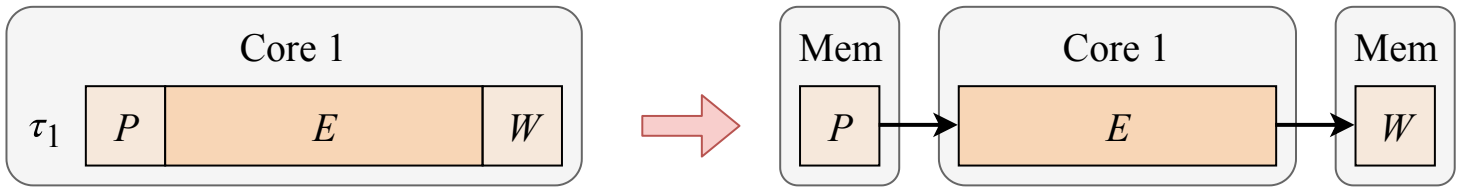


Up to 40% gain!

Schedulability analysis

Yao et al. 2016 validation

From PEW-tasks to distributed tasks



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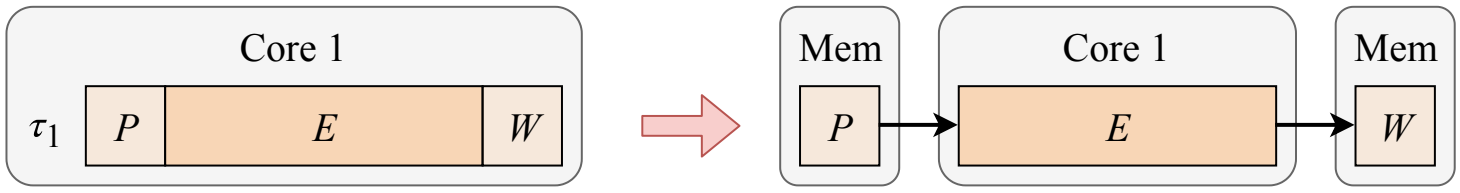


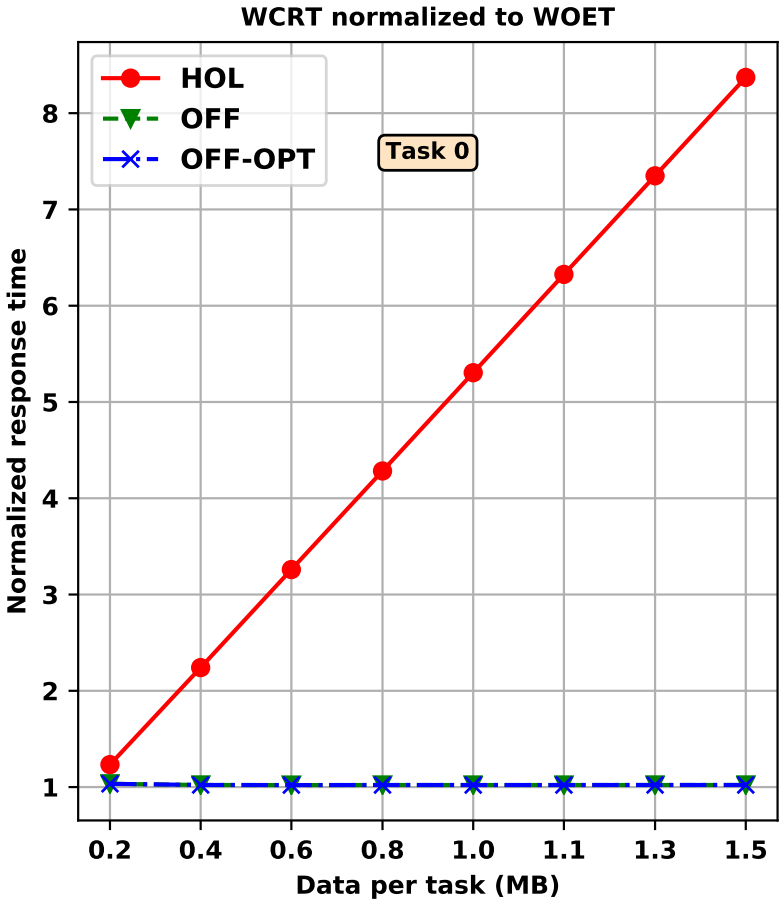
MAST tool

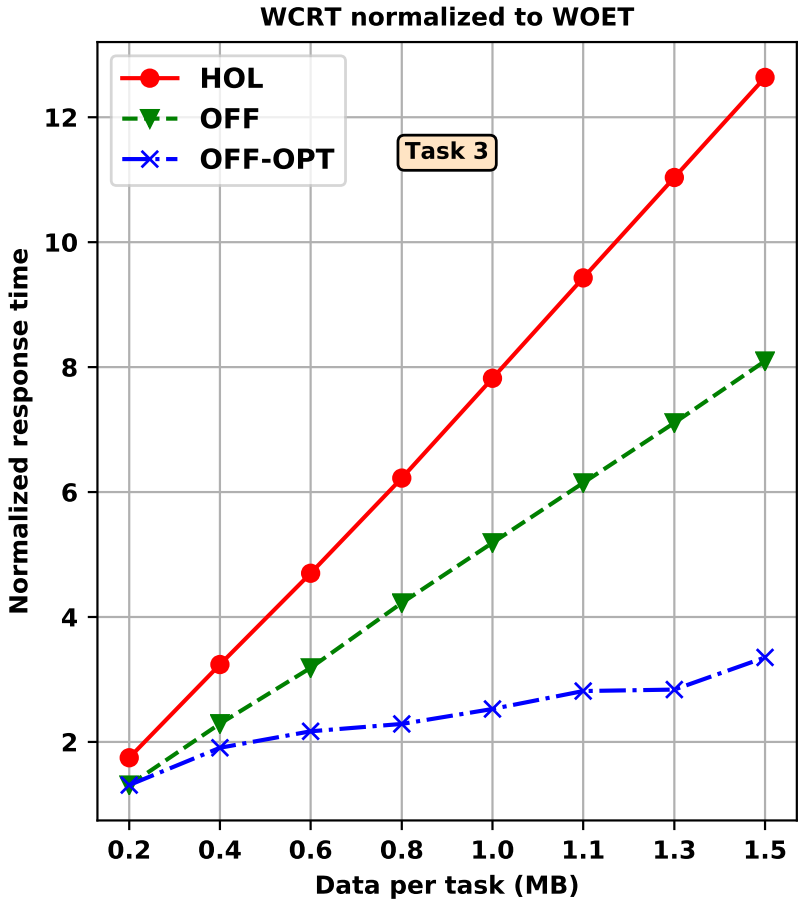
`mast.unican.es`

+

- Hollistic
- Offset
- Offset-optimised

Practical results





Paper's details

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Abstract

The demands for high performance computing with a low cost and low power consumption are driving a transition towards multi-core processors in many consumer and industrial applications. However, the adoption of multi-core processors in the domain of real-time systems faces a series of challenges that has been the focus of great research intensity during the last decade. These challenges arise in great part from the non real-time nature of the hardware arbiters that schedule the access to shared resources, such as the main memory. One solution proposed in the literature is called Memory Centric Scheduling, which defines a separate software scheduler for the sections of the tasks that will access the main memory, hence circumventing the low level unpredictable hardware arbiters. Several Memory Centric schedulers and associated theoretical analyses have been proposed, but as far as we know, no actual implementation of the required OS-level underpinnings to support dynamic event-driven Memory Centric Scheduling has been presented before. *In this paper* we aim to fill this gap, targeting cache based COTS multi-core systems. We will confirm via measurements the main theoretical benefits of Memory Centric Scheduling (e.g. task isolation). Furthermore, we will describe an effective schedulability analysis using concepts from distributed systems.

2012 ACM Subject Classification Computer systems organization → Real-time systems

Keywords and phrases real-time, multi-core, memory centric, predictability, implementation, rtos

Digital Object Identifier 10.4230/LIPIcs.ECRTS.2019.1

Funding *Juan M. Rivas*: This research was funded by Wallonia Region (Belgium) BEWARE grant PARTITA (1610375)

1 Introduction

Advancements in the manufacturing process of integrated electronics, in addition to the sheer size of the general computing market, are increasingly widening the offer and lowering the costs of commercial off-the-shelf (COTS) multi-core processors. While these commercial processors are generally designed with *average* performance in mind, their wide availability and low cost are pushing their adoption into real-time applications where a different set of requirements such as predictability and worst-case guarantees are needed.

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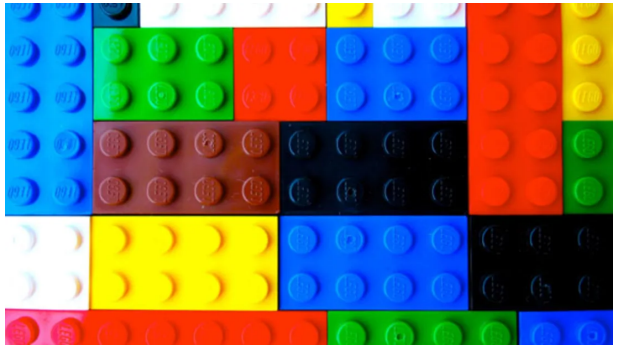

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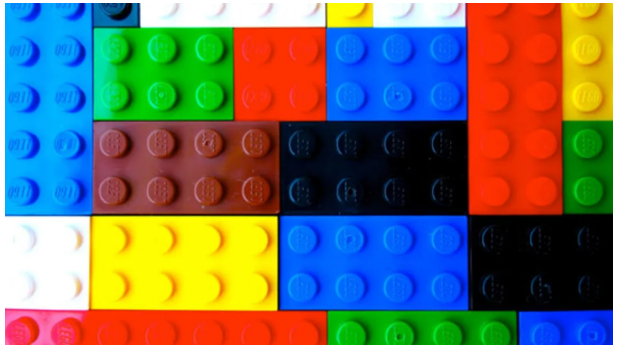

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        memphase_end();
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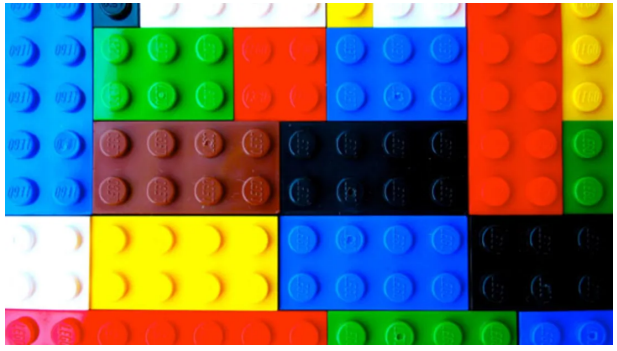

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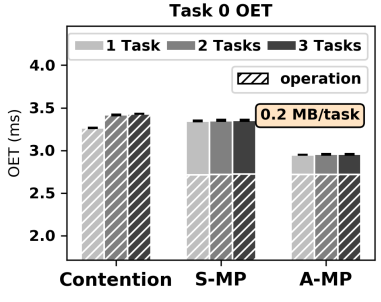

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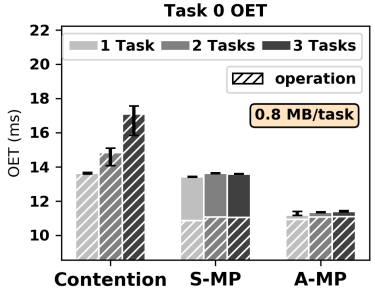

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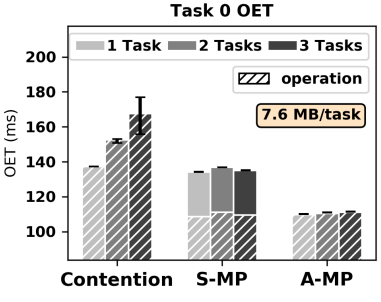
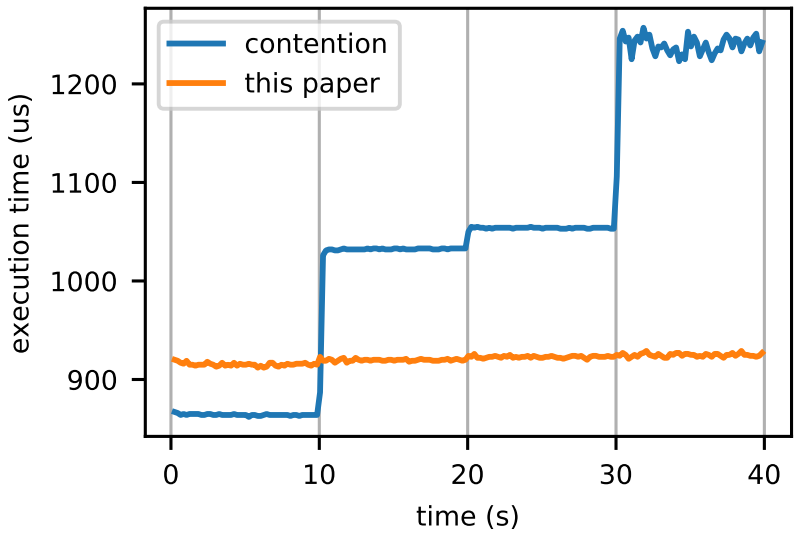


(c)

Conclusion


contention
this paper
execution time (us)
1200
1100
1000
900
0
10
20
30
40
time (s)

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